Enhancing SRAM Performance by Advanced FinFET Device and Circuit Technology Collaboration for 14nm Node and Beyond

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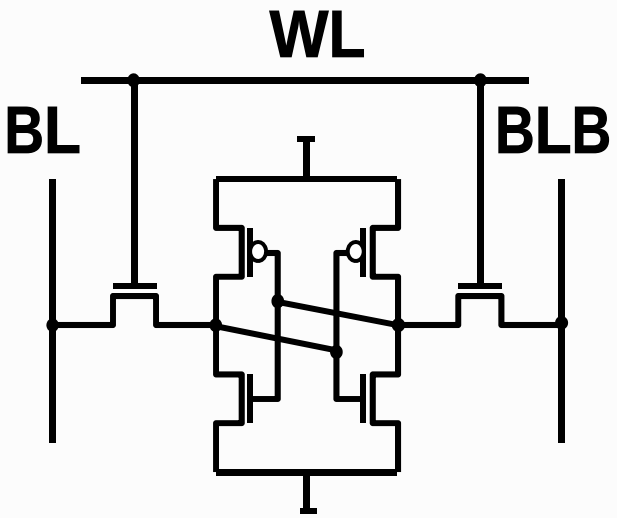
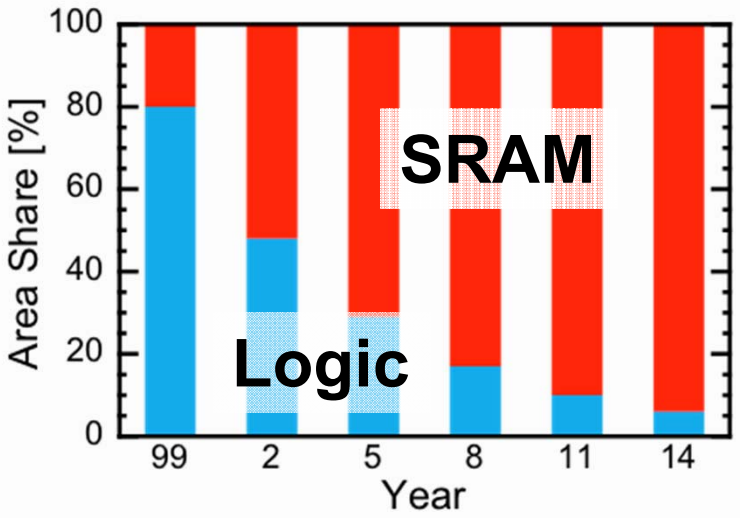
Nanoelectronics Res. Inst.

National Institute of AIST

Background





Area Share of the embedded SRAM

Issues in SRAM Cell Scaling

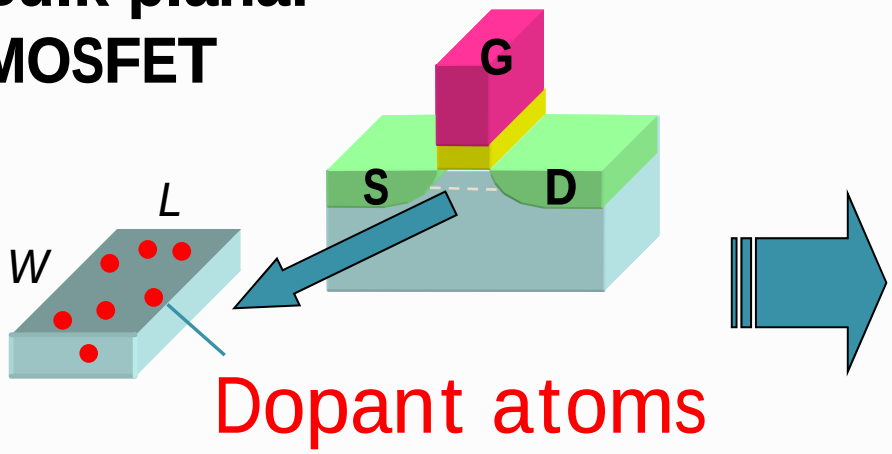
- ✓Rapid increase of stand-by leakage
- ✓Yield reduction due to V_{th} variation

FinFET SRAM

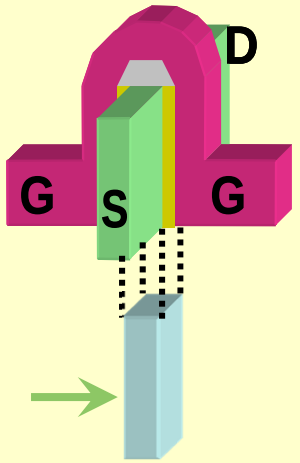
Merit of FinFET in SRAM Cell

- ✓Short Channel Effect Immunity
- ✓Less V_{th} variability expected

Bulk planar MOSFET

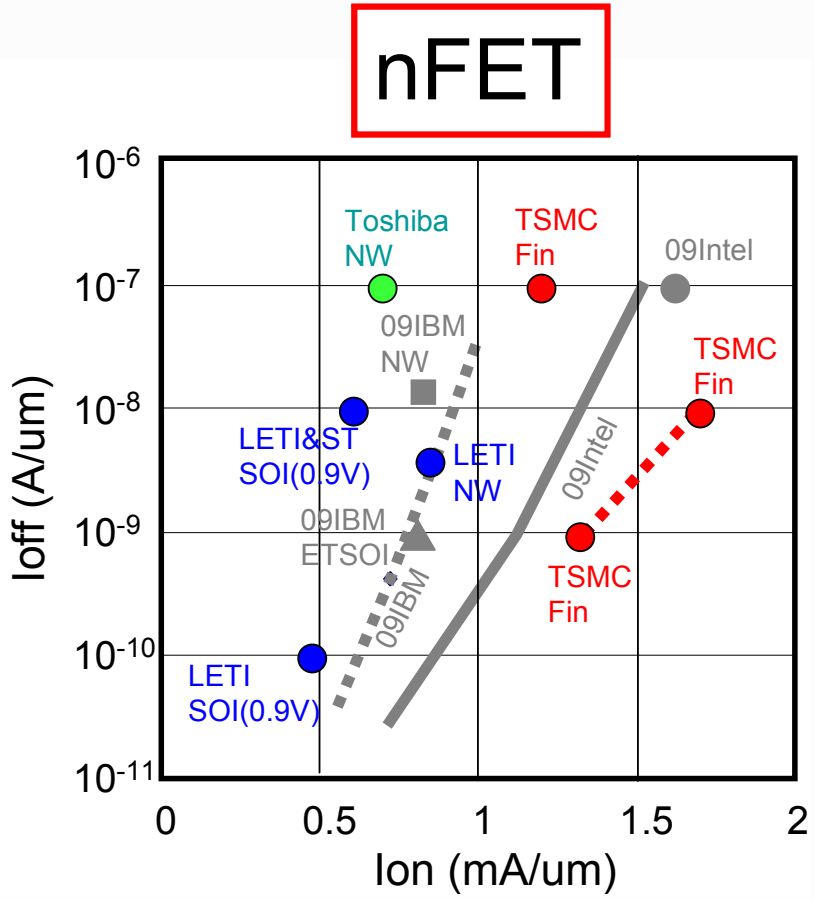


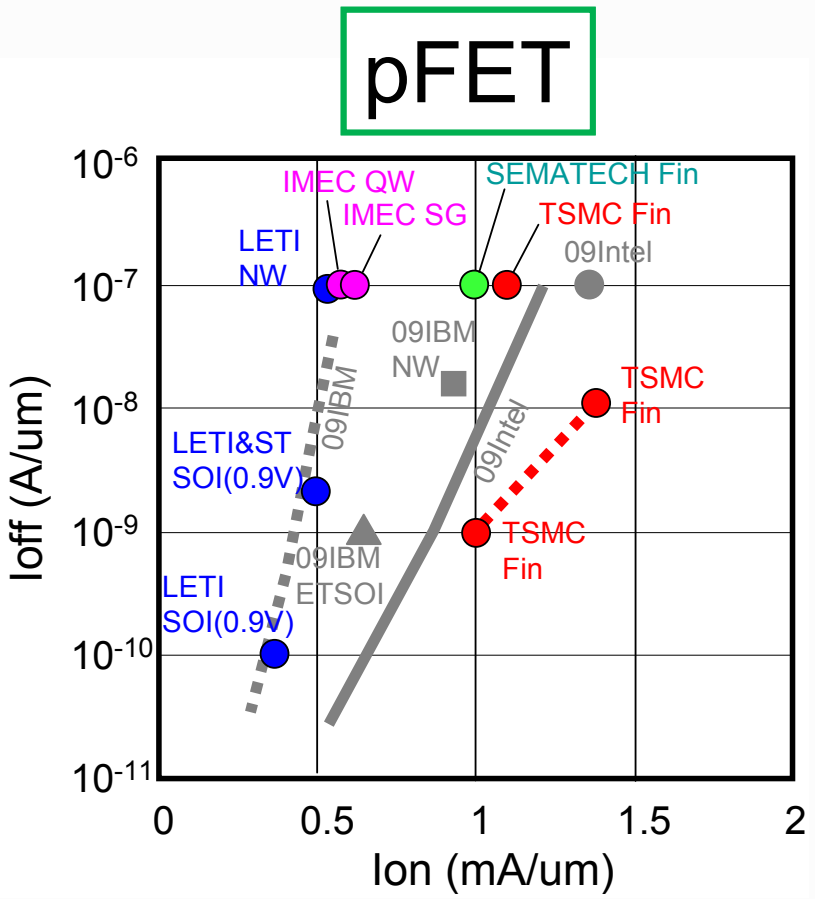
FinFET



Undoped channel

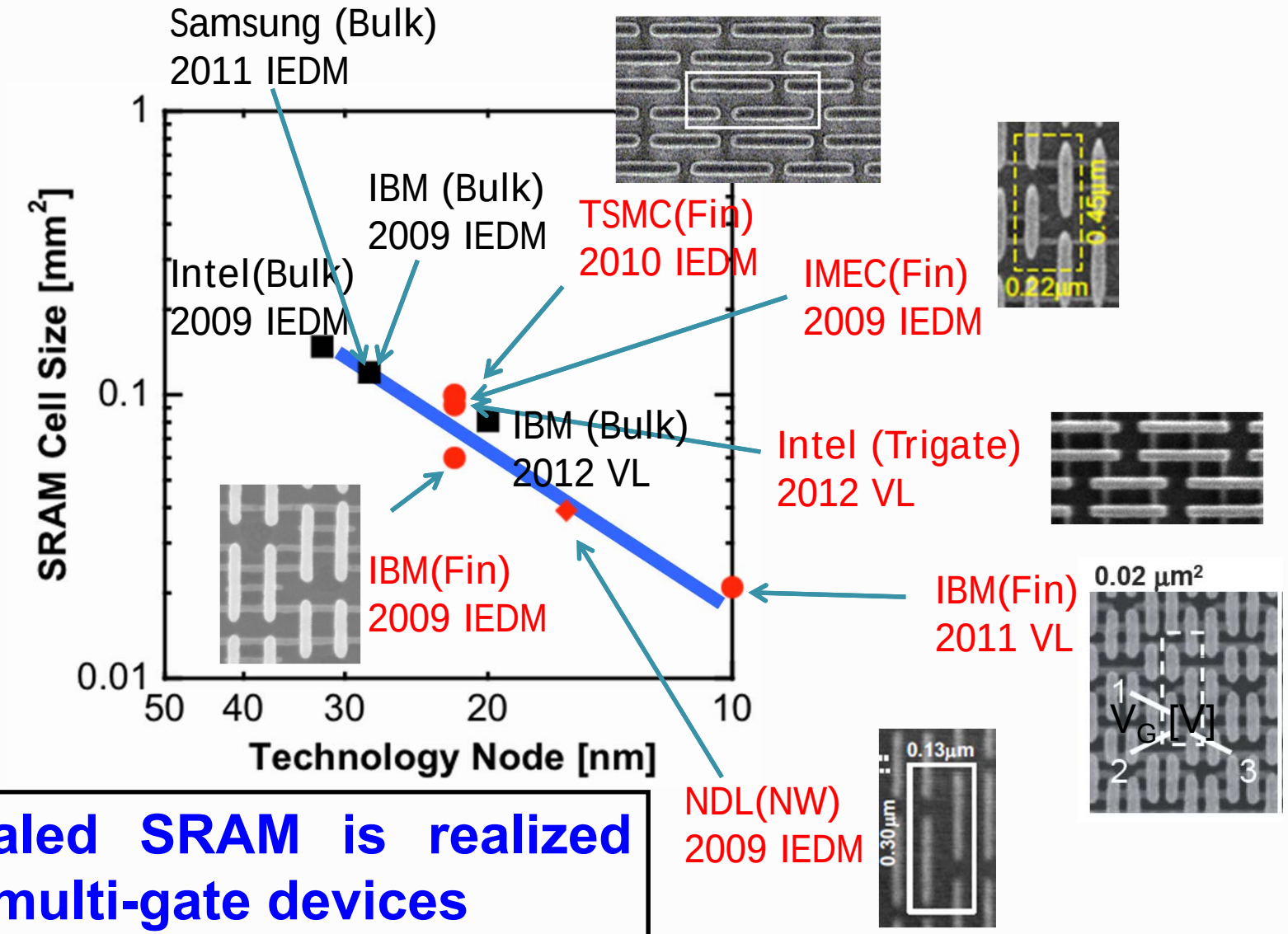
On-Current Benchmark





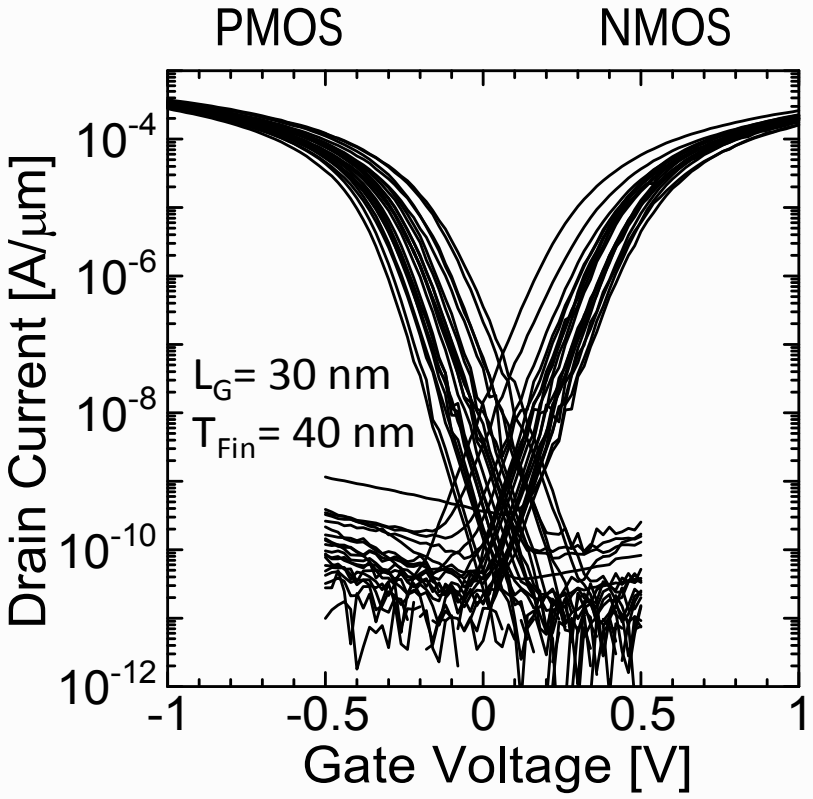
✓**FinFET exhibits the highest performance**

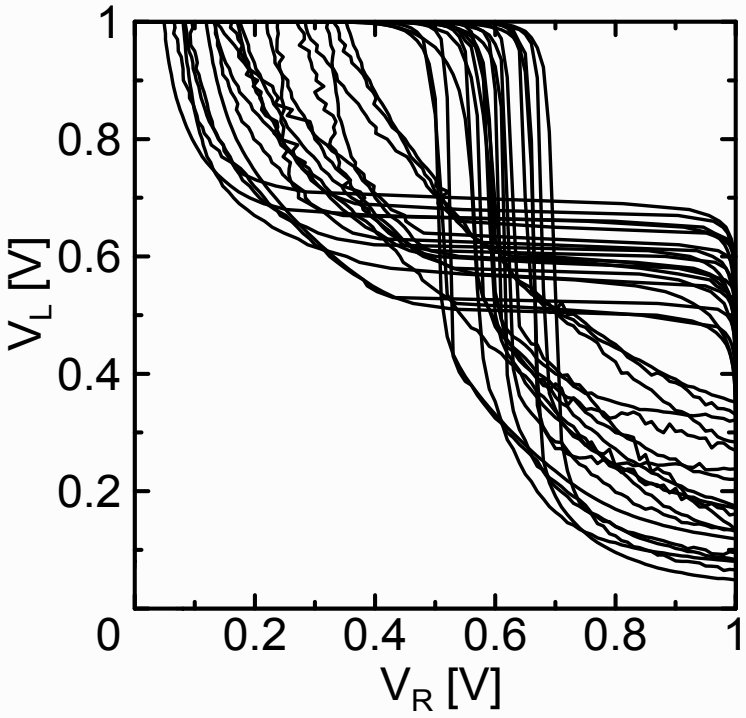
SRAM Benchmark



✓**Scaled SRAM is realized by multi-gate devices**

FinFET IV Curves with Variability





- **Fluctuation of V_{th} exist even for the undoped channel FinFET.**
- **Stability of the SRAM cell is reduced due to variability.**

Outline

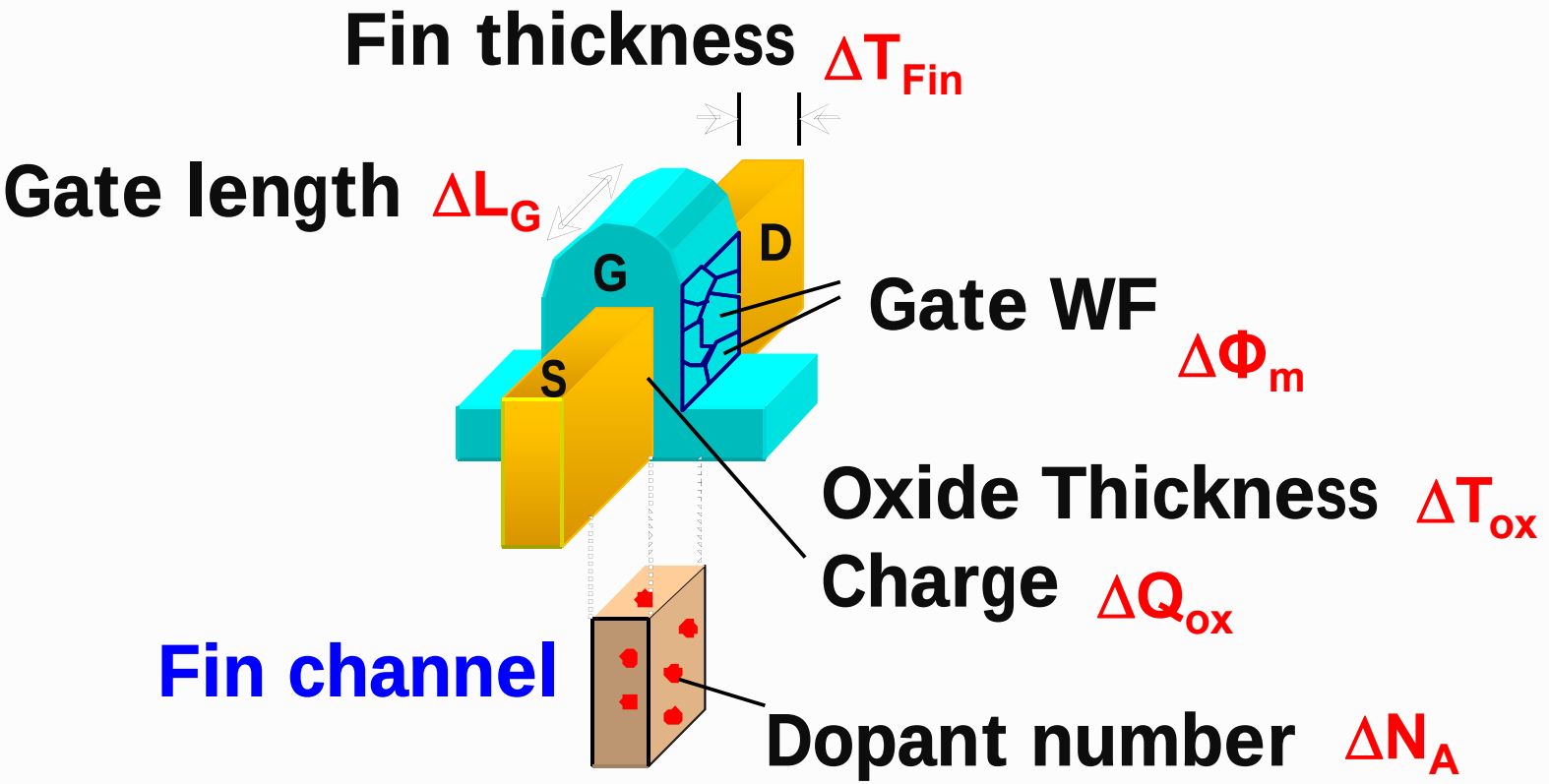
Device and Circuit Collaboration for the FinFET SRAM

1. Device Approach for Suppressing Variability
   - Variability Analysis
   - Variability Reduction Process
2. Circuit Approach for Enhancing SRAM Stability
   - Independent-DG FinFET
   - Flex-Vth SRAM, Flex-PG SRAM
   - Dynamic PG Control SRAM
   - Fin Height Control SRAM
3. Future Prediction by the Device and Circuit Technology Collaboration

Device Approach for Suppressing Variability

FinFET Variability Analysis

V_{th} Variation Sources



Analytical Method

Variance (σ^2) of Vt : sum of each component

$$\sigma_{Vt}^{\ 2} = \left(\frac{\partial Vt}{\partial Lg}\sigma_{Lg}\right)^2 + \left(\frac{\partial Vt}{\partial Tfin}\sigma_{Tfin}\right)^2 + \left(\frac{\partial Vt}{\partial Tox}\sigma_{Tox}\right)^2 + \left(\frac{\partial Vt}{\partial \Phi_m}\sigma_{\Phi m}\right)^2$$

Dimension variation sources

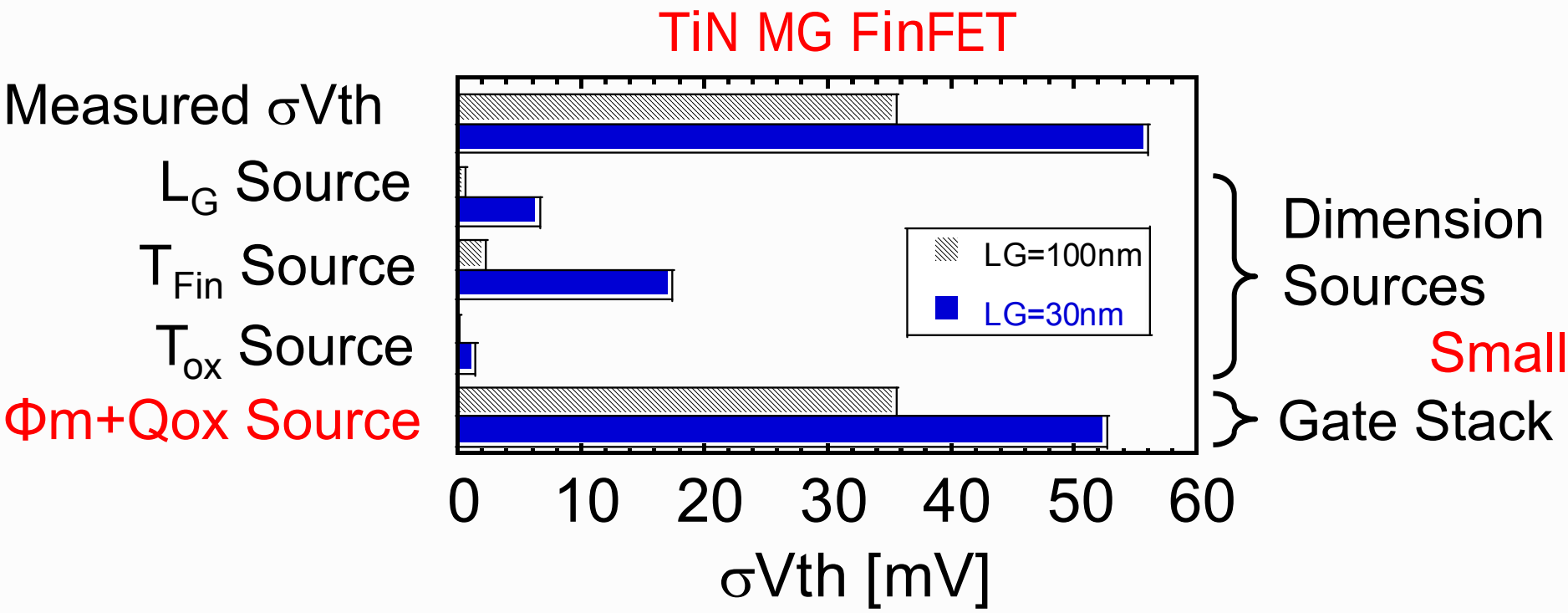
WFV+Qox source

$$+\left(\frac{\partial Vt}{\partial N_A}\sigma_{NA}\right)^2$$

Dopant source

S. Ouchi et al. (AIST), IEDM 2008
T. Matsukawa et al. (AIST), VLSI 2009

Contribution of Vth Variability

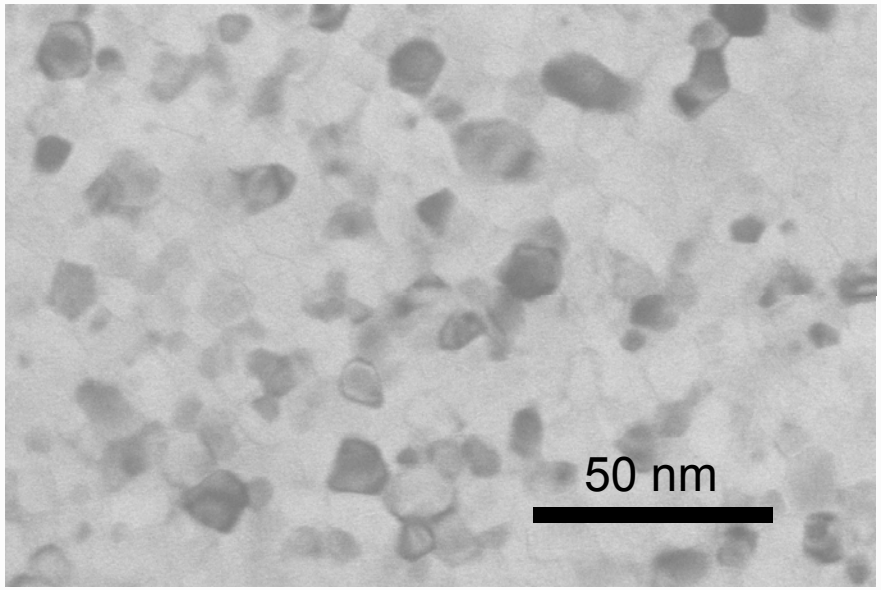


⇨ **Dimension variation sources are small**
Main component is gate-stack variation

K. Endo (AIST), EDL 2010

Origin of the WFV

Plane TEM image of the TiN film



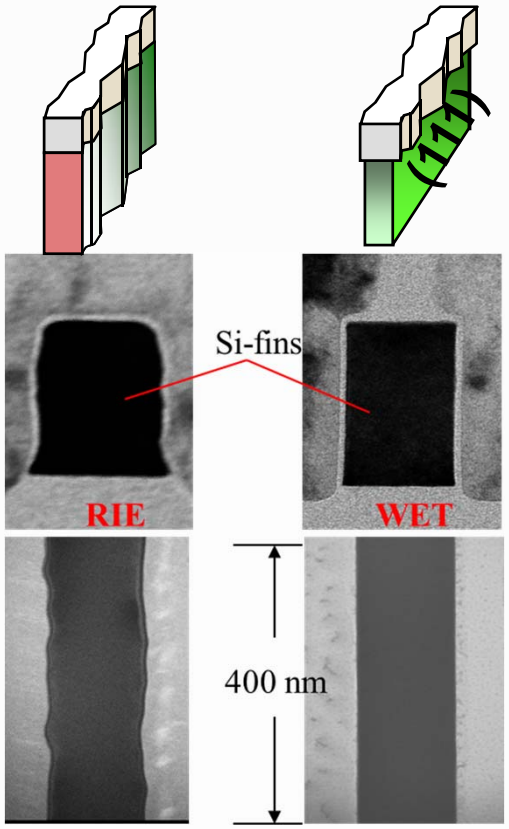
Orientation Dependent WF for TiN

<100> 4.6 eV
<111> 4.4 eV

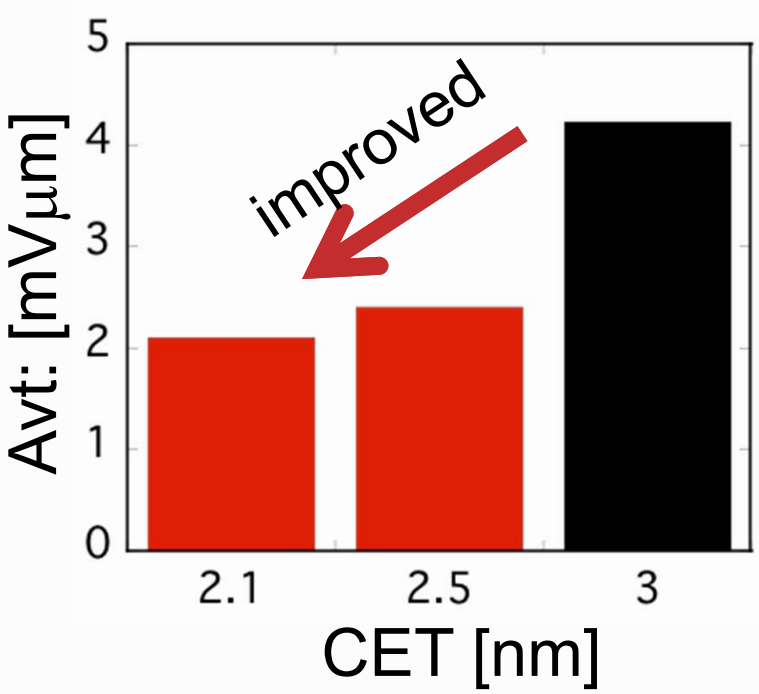
- ✓**Grain size of MG's is comparable to scaled L_G**
- ✓**Grains with different orientation causes WFV**

WFV Reduction by Channel Smoothing

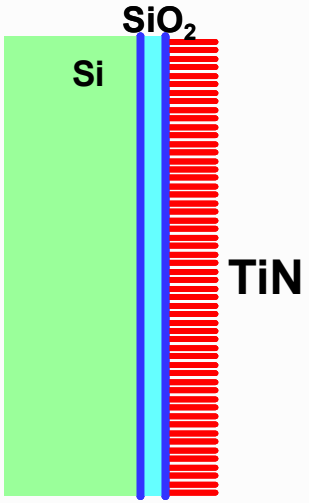
Y.X.Liu, (AIST) VLSI, 2010, p.101



Nano Wet etching (NWE)



Avt: Slope of Pelgrom Plot



Uniformly Aligned Metal

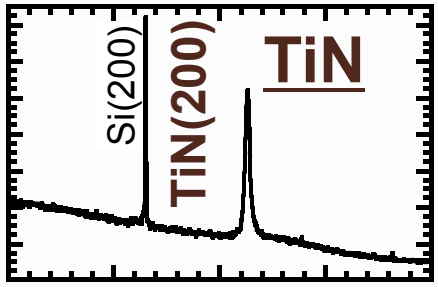
✓ WFV is reduced due to uniformly aliened metal

Reducing WFV: Amorphous Metal-Gate

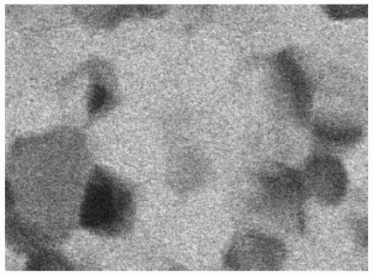
TiN film (Ref.)

Sputtering
Ti target
Ar/N_2 gas

XRD (post RTA)



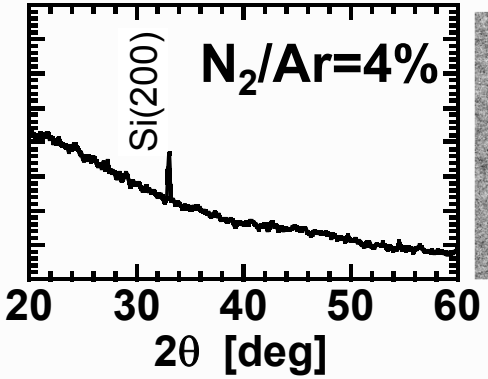
Plane view TEM (post RTA)

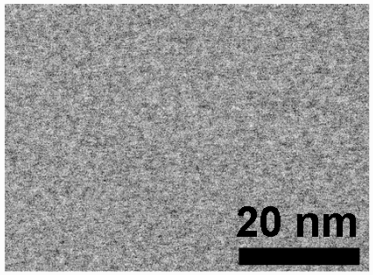


Poly-crystal

TaSiN film

Sputtering
$TaSi_2$ target
Ar/N_2 gas



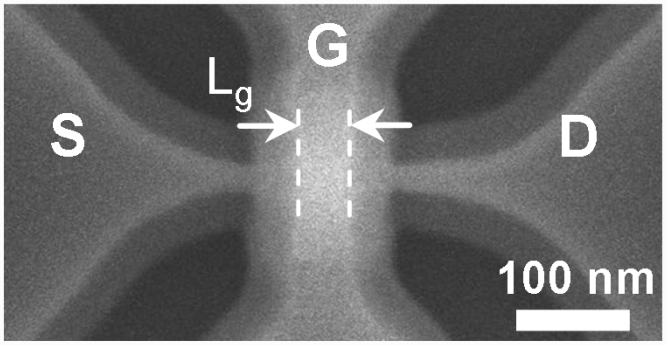


Amorphous

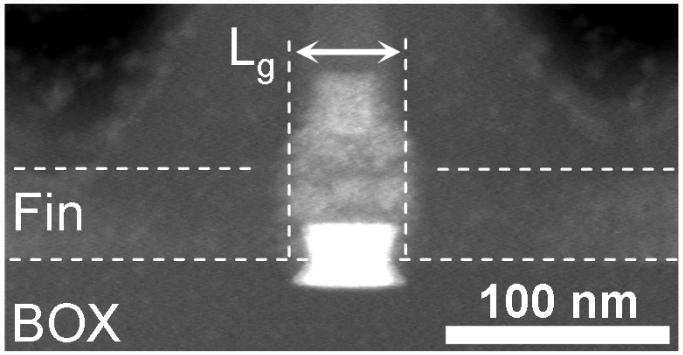
T. Matsukawa, et al., (AIST)
IEDM, 2012, p.175.

The FinFET with the TaSiN MG

Top view SEM
(aft. spacer formation)

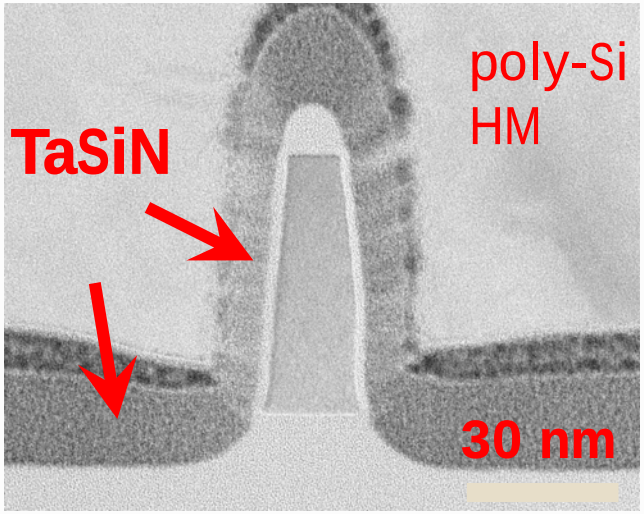


Gate cross section TEM



Designed L_g~50 nm

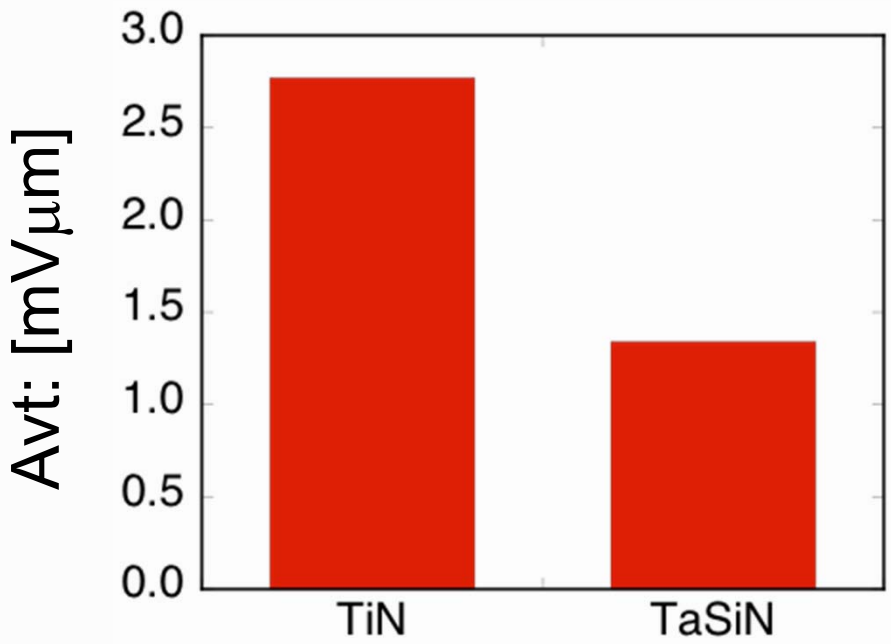
Fin channel
cross section TEM



Conformal TaSiN MG is formed

T. Matsukawa, et al., (AIST) , IEDM, 2012, p.175.

Reduction of Vth Variation

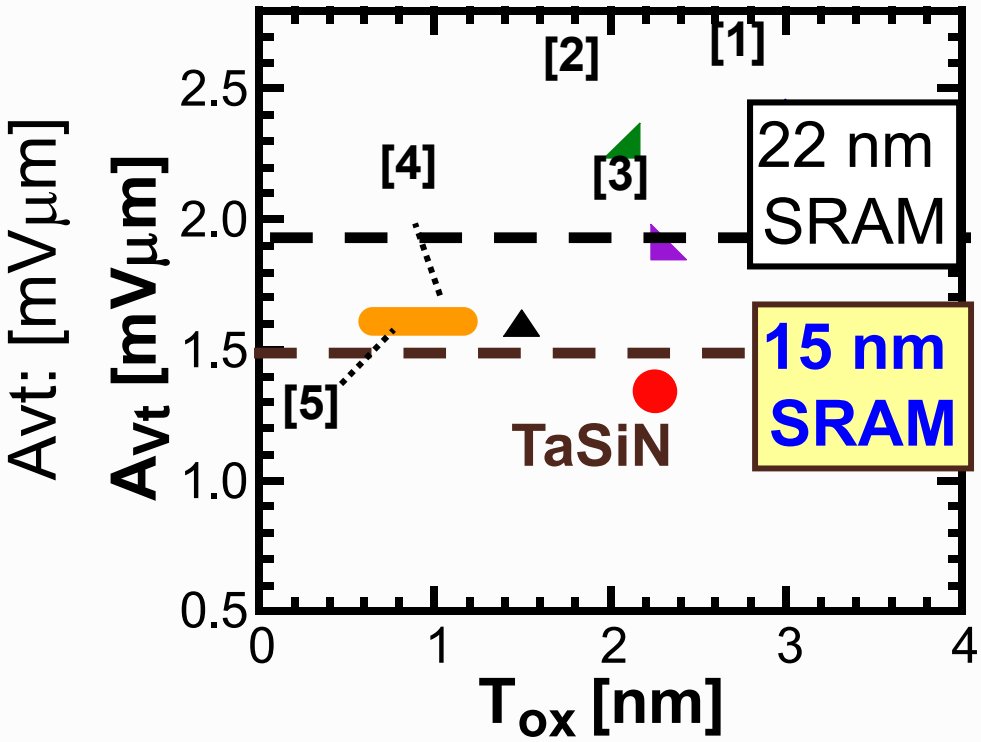


Avt: Slope of Pelgrom Plot

TaSiN gate shows smallest A_{Vt} of 1.34mVμm

T. Matsukawa, et al., (AIST) , IEDM, 2012, p.175.

Benchmark of Avt



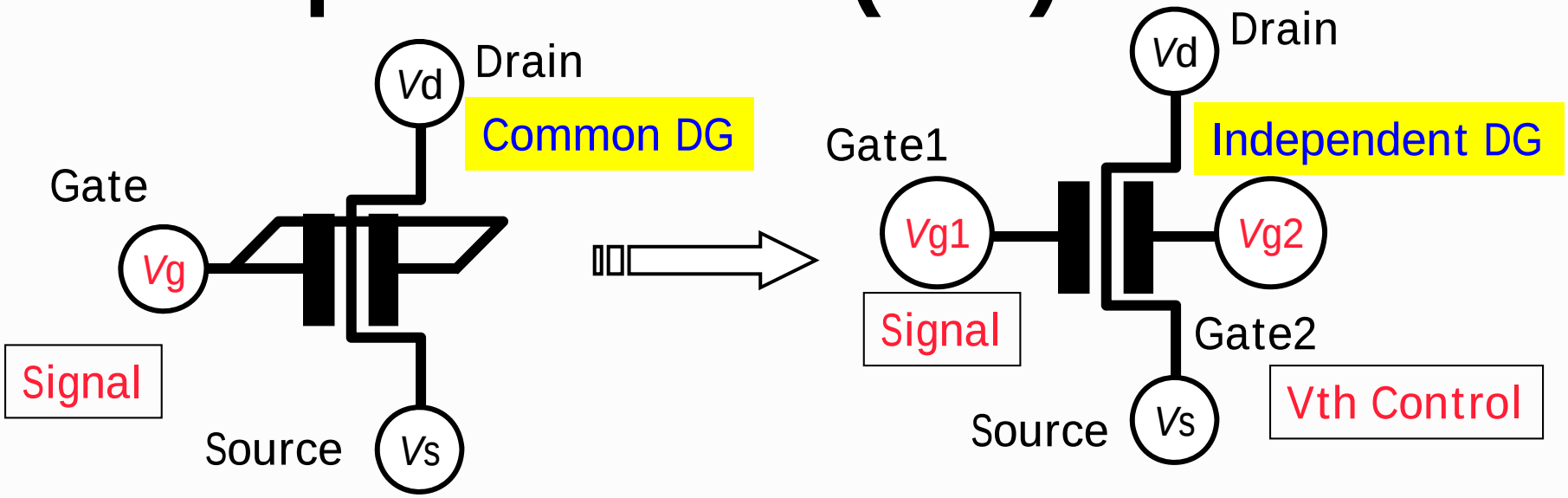
References of A_{Vt}

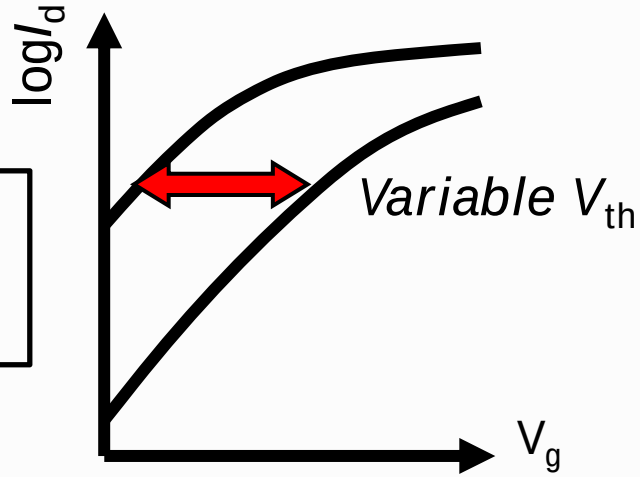
[1] ***AIST, 2009***
[2] ***IMEC, 2008***
[3] ***AIST, 2010***
[4] ***IMEC, 2010***
[5] ***IBM/GF, 2012***

T. Matsukawa, et al., (AIST) , IEDM, 2012, p.175.

Circuit Approach to Enhance SRAM Stability

Independent-DG (IDG) FinFET

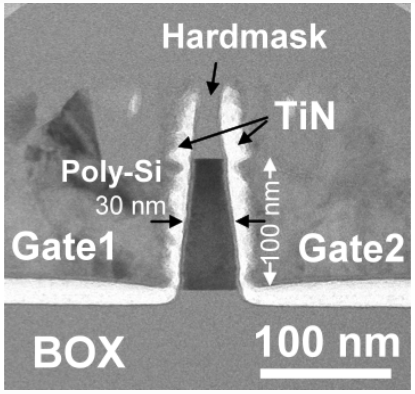


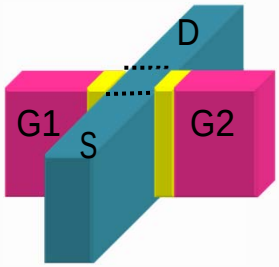


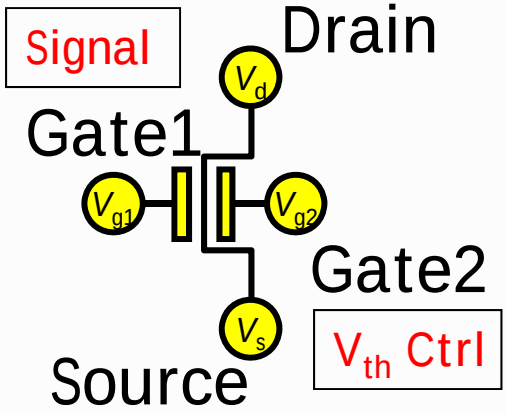
- ✓Common-DG: Fixed Vth
- ✓Independent-DG: Variable Vth

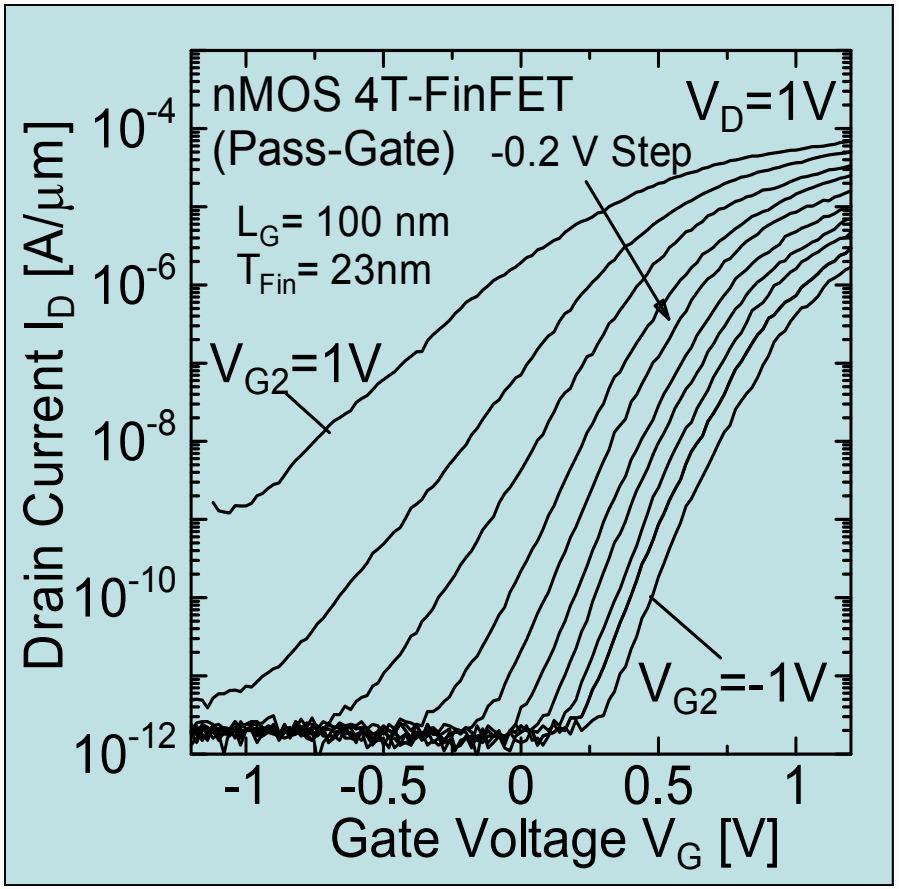
Y. X. Liu et al. (AIST) IEDM 2003

IDG-FinFET Example





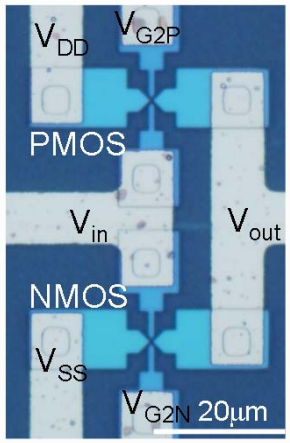




K. Endo et al. (AIST), IEEE EDL 2007

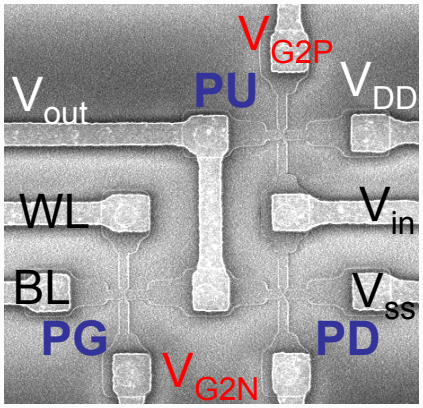
IDG-FinFET CMOS Circuits

CMOS Inverter



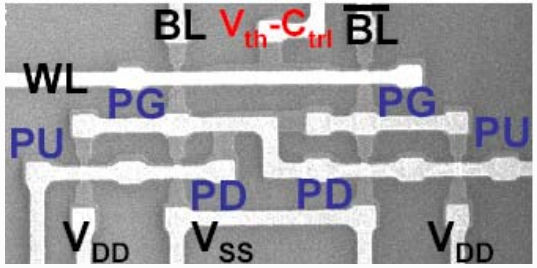
K.Endo (AIST), EDL 2007

Flex-V_{th} SRAM



K.Endo (AIST), IEDM 2008
EDL 2009

Flex-PG SRAM
Dynamic PG Control



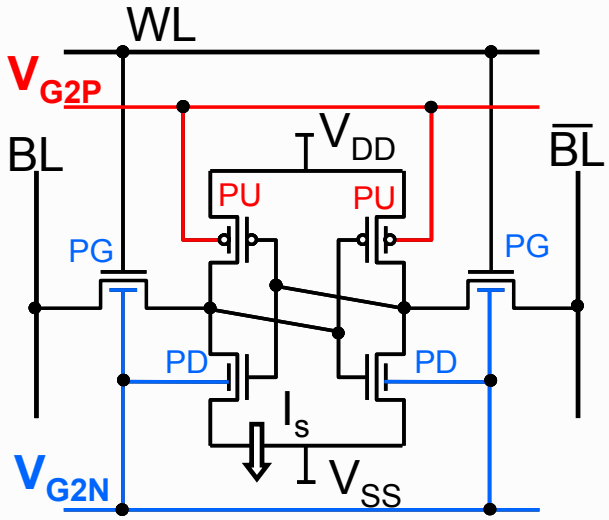
S. O'uchi (AIST), CICC 2007
ESSCIRC 2010
IEDM 2008

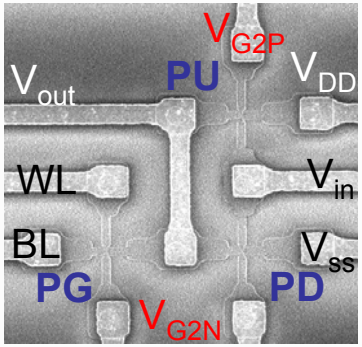
K. Endo (AIST), ESSDERC2008
IEDM 2008

V_{th} control of all Tr.
Reduction of leakage current

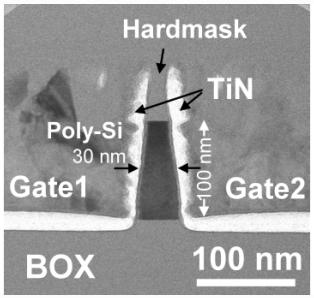
V_{th} control of pass-gate
Enhancing SNM

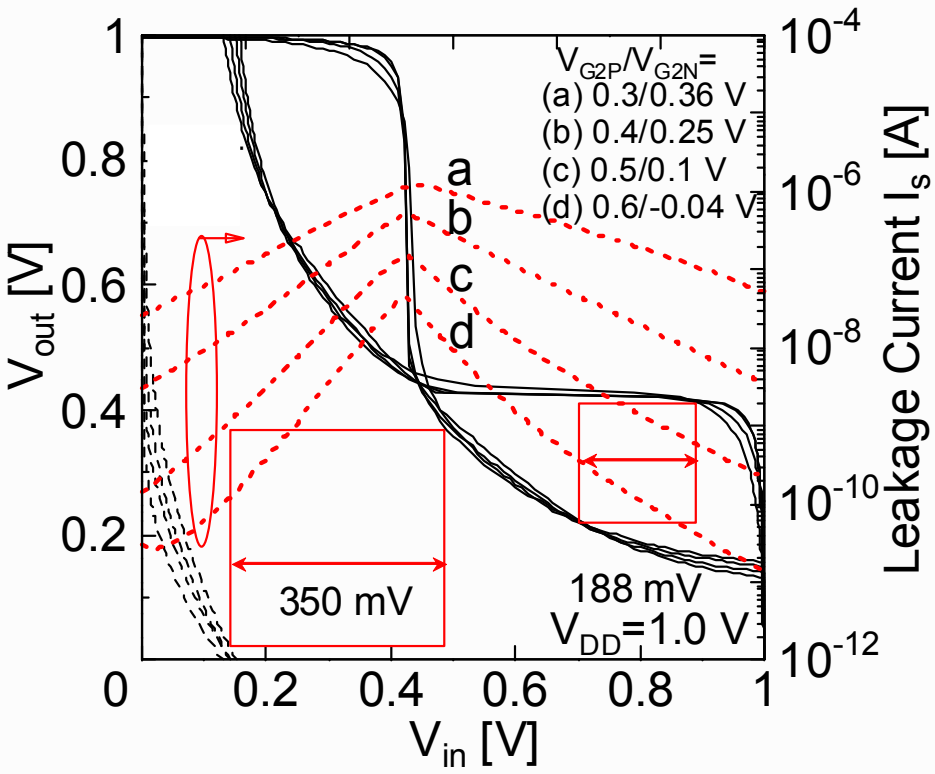
Flex-Vth SRAM Cell





CDG-FinFET

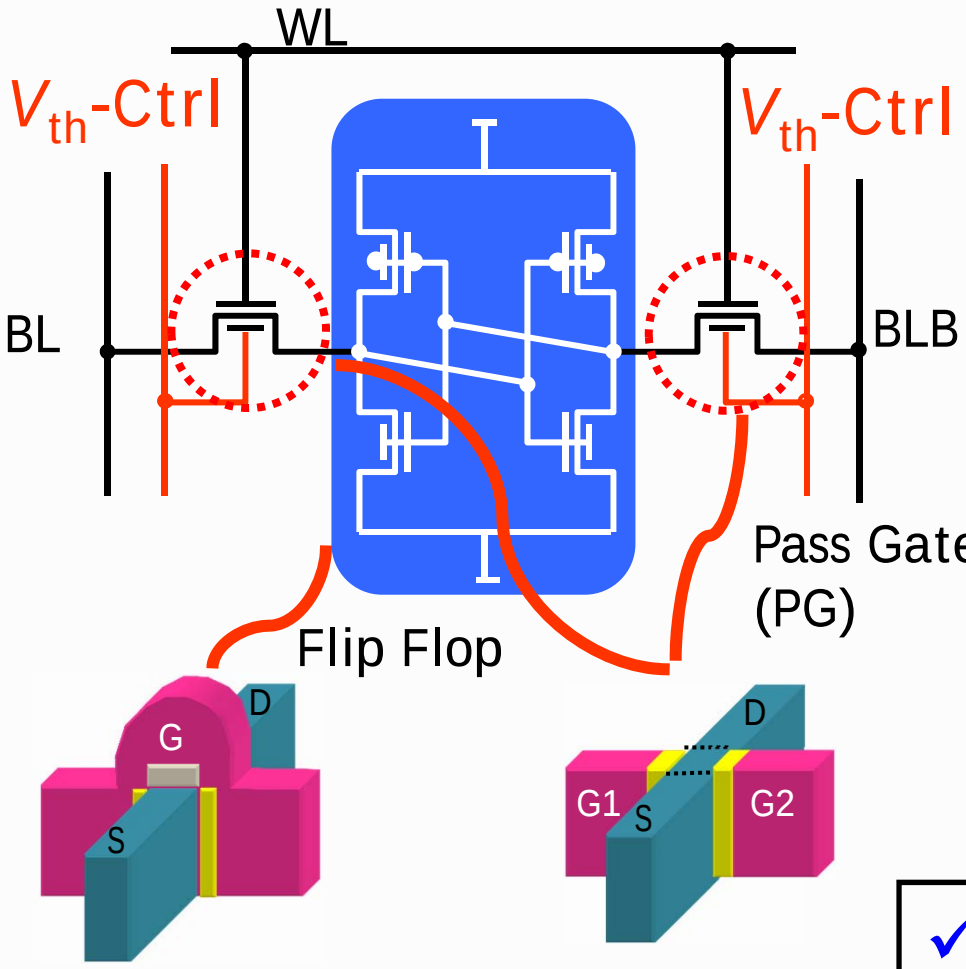


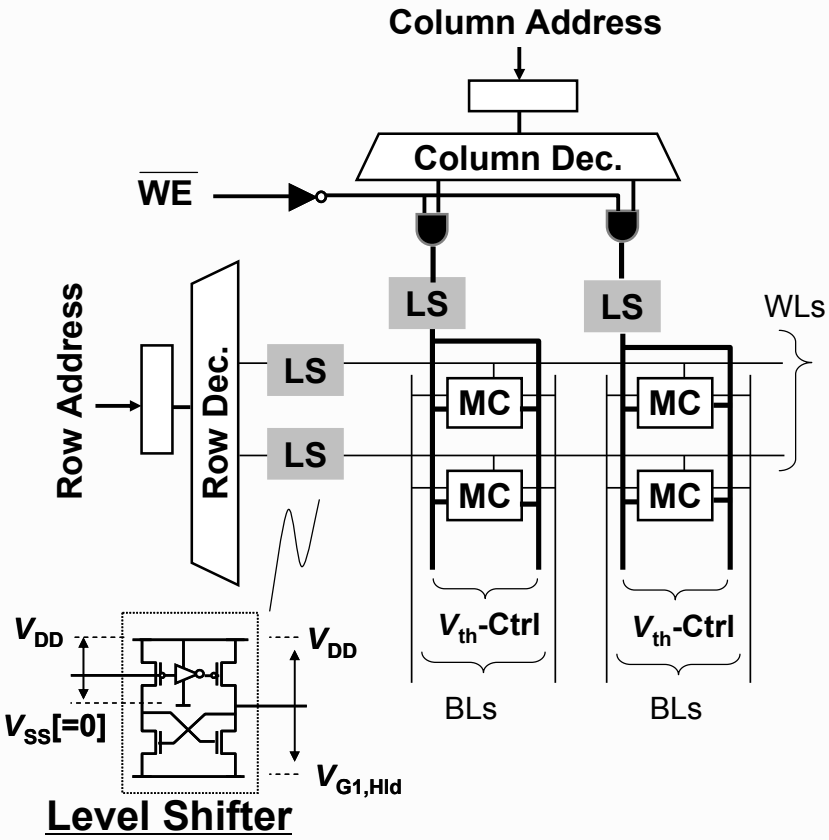


K. Endo et al. (AIST), IEDM 2008

Active and stand-by leaks are controlled with the same SNM

Flex-Pass-Gate (PG) SRAM Cell

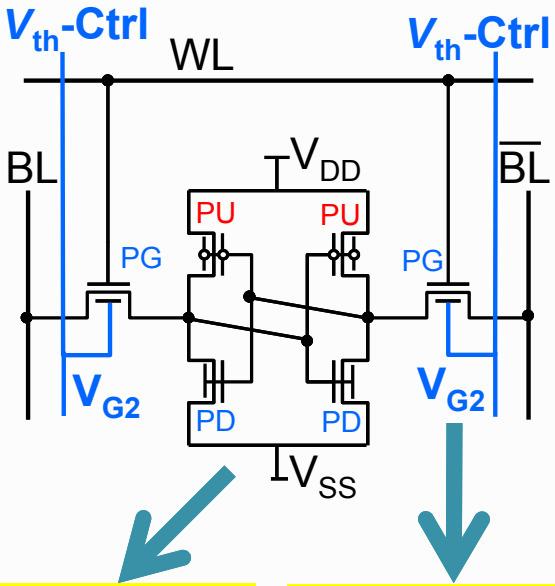




S. O'uchi et al. (AIST), 2007 IEEE CICC

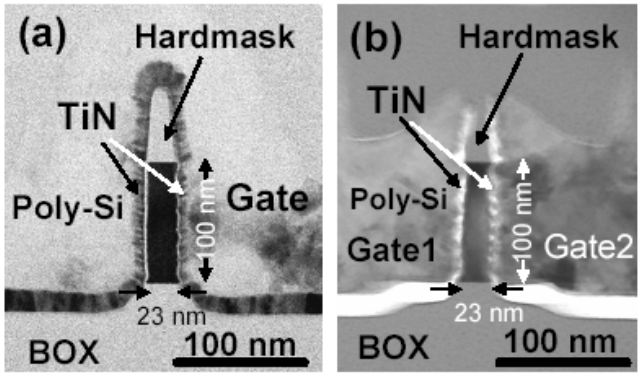
✓ **Vth control of the PG enhances noise margin**

Flex-PG SRAM Cell Results

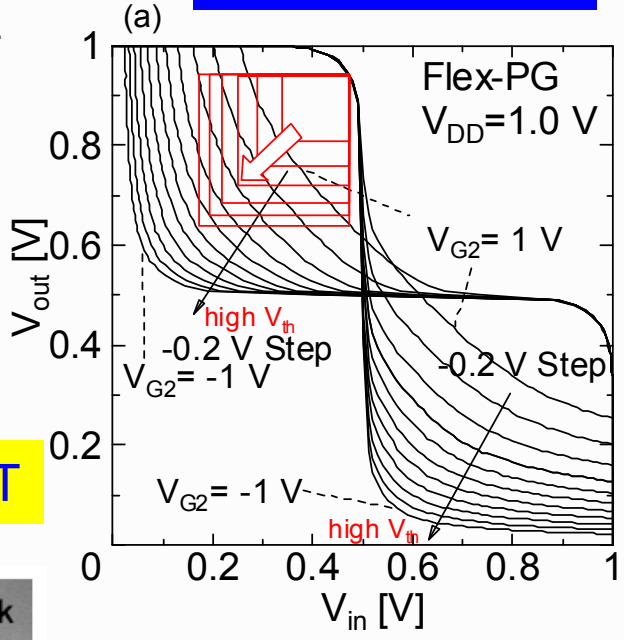


CDG-FinFET

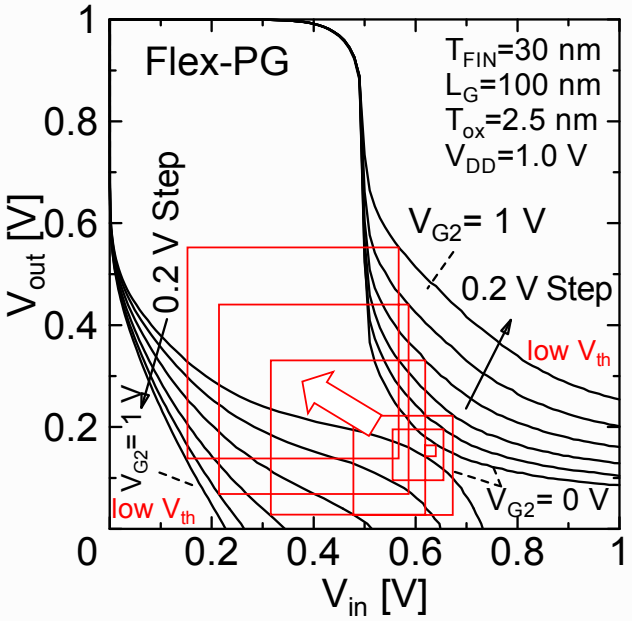
IDG-FinFET



Read Margin



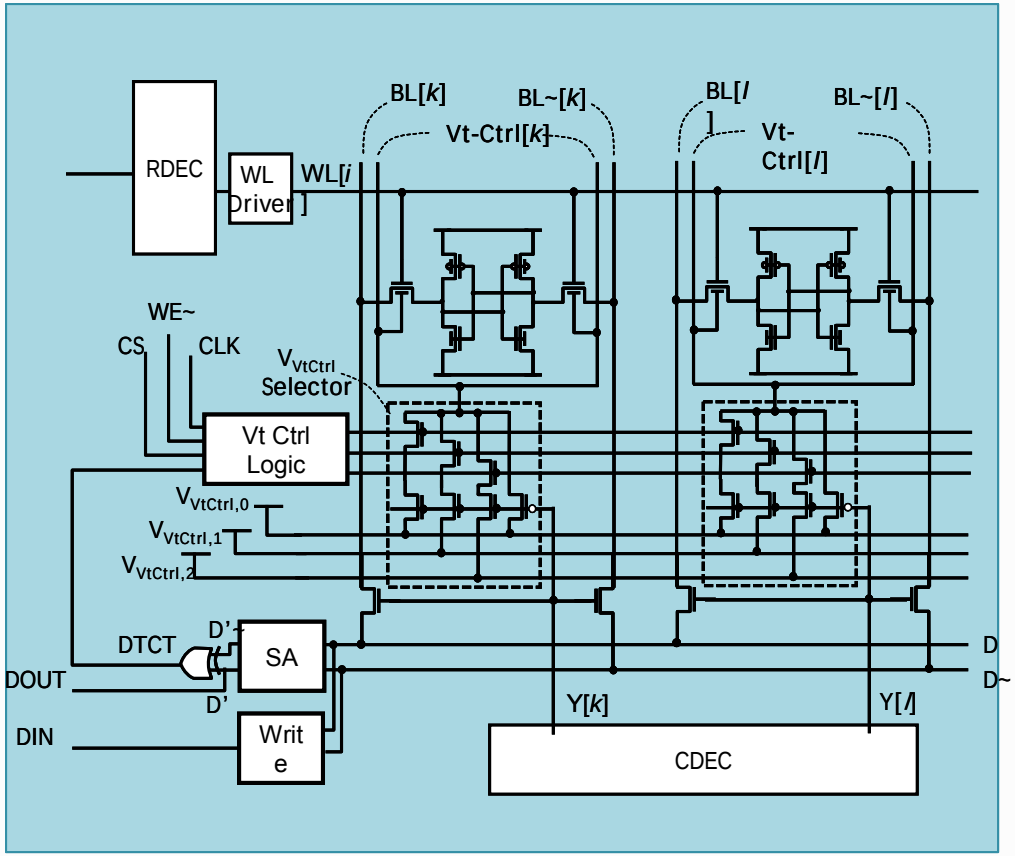
Write Margin

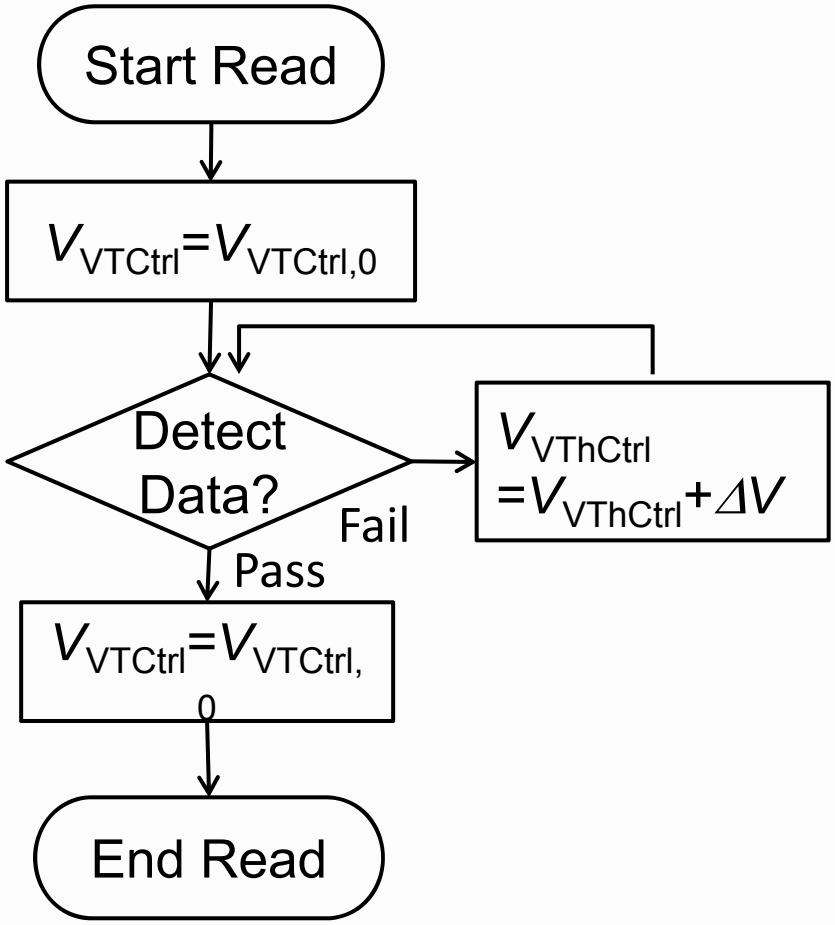


- ✓**Flexible noise margin control is successfully demonstrated.**
- ✓**Both RM and WM are enhanced.**

K. Endo et al. (AIST), IEDM 2008, ESSDERC 2008

Dynamic PG Control Algorithm

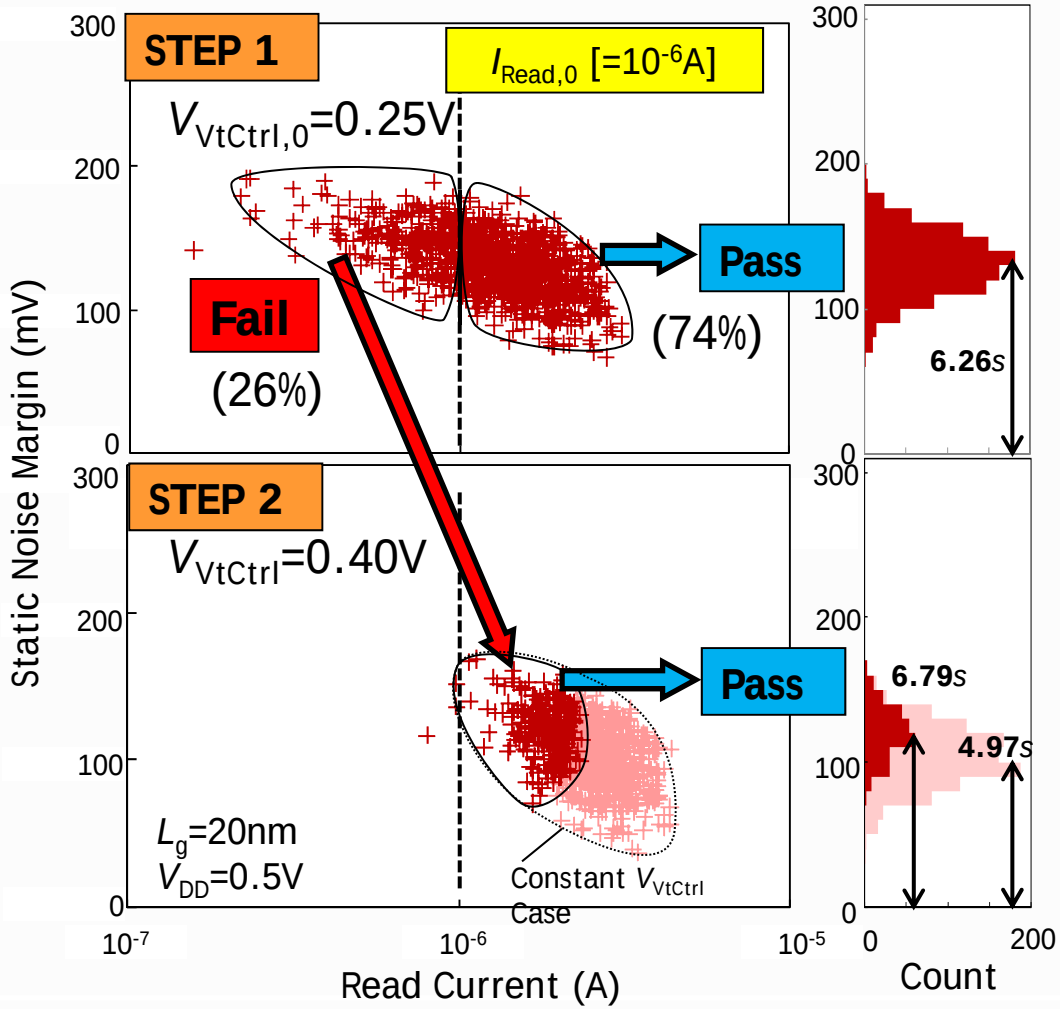




The optimal bias is found for each cell and the instability is avoided.
Read speed reduction is avoided.

S. O'uchi et al. (AIST), ESSCIRC 2010,474

Dynamic PG Control Results



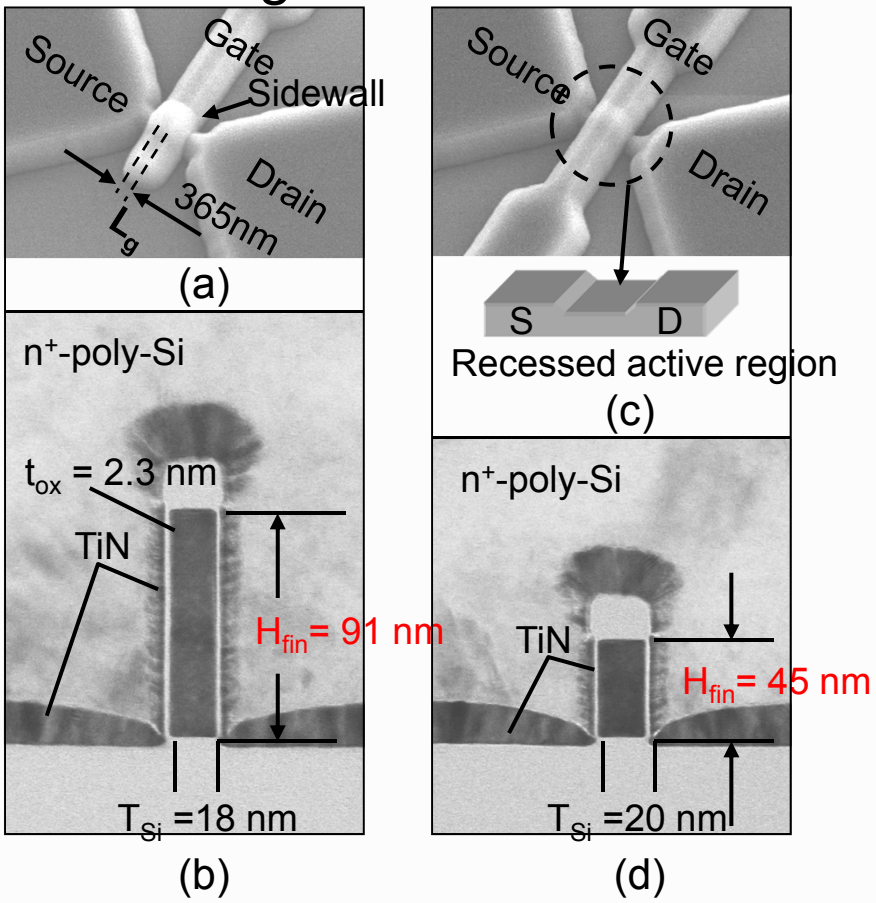
20-nm-L_G technology
V_{DD} = 0.5V

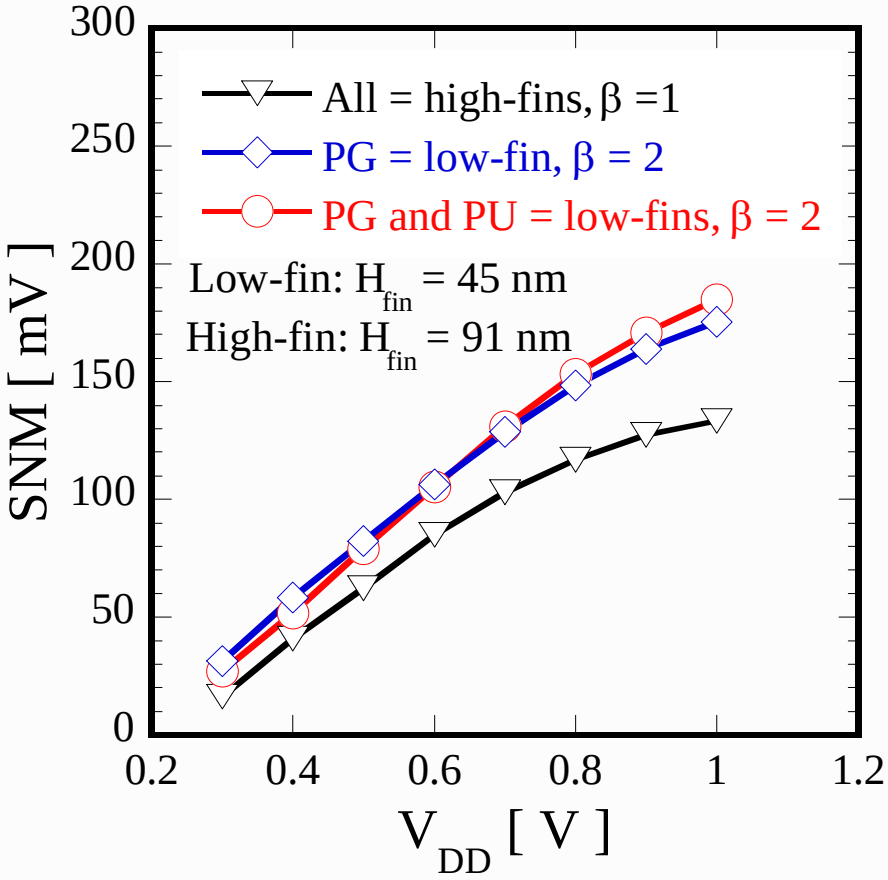
✓ **2 step read keeps 6-sigma tolerance of SNM**

S. O'uchi et al. (AIST), ESSCIRC 2010,474

Fin Height Control SRAM

PD with a high-fin PG with a low-fin





Fin height control enhances SNM

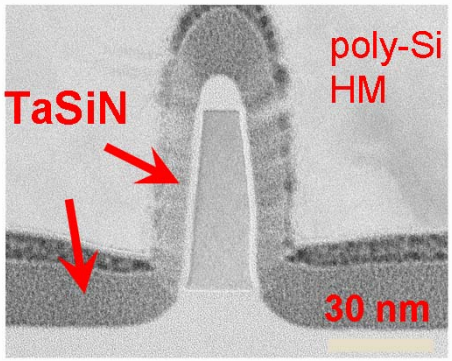
Y. Liu et al. (AIST), ESSDERC 2010

Future Prediction by the Device and Circuit Technology Collaboration

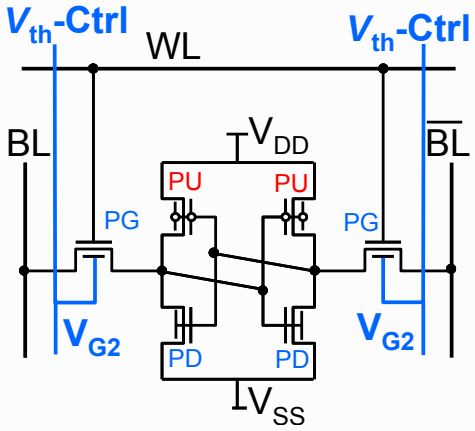
Simulated SRAM Cell

- ✓TaSiN amorphous metal-gate (A_{VT} 1.34)
- ✓Flex-PG Technology for enhancing SNM

TaSiN

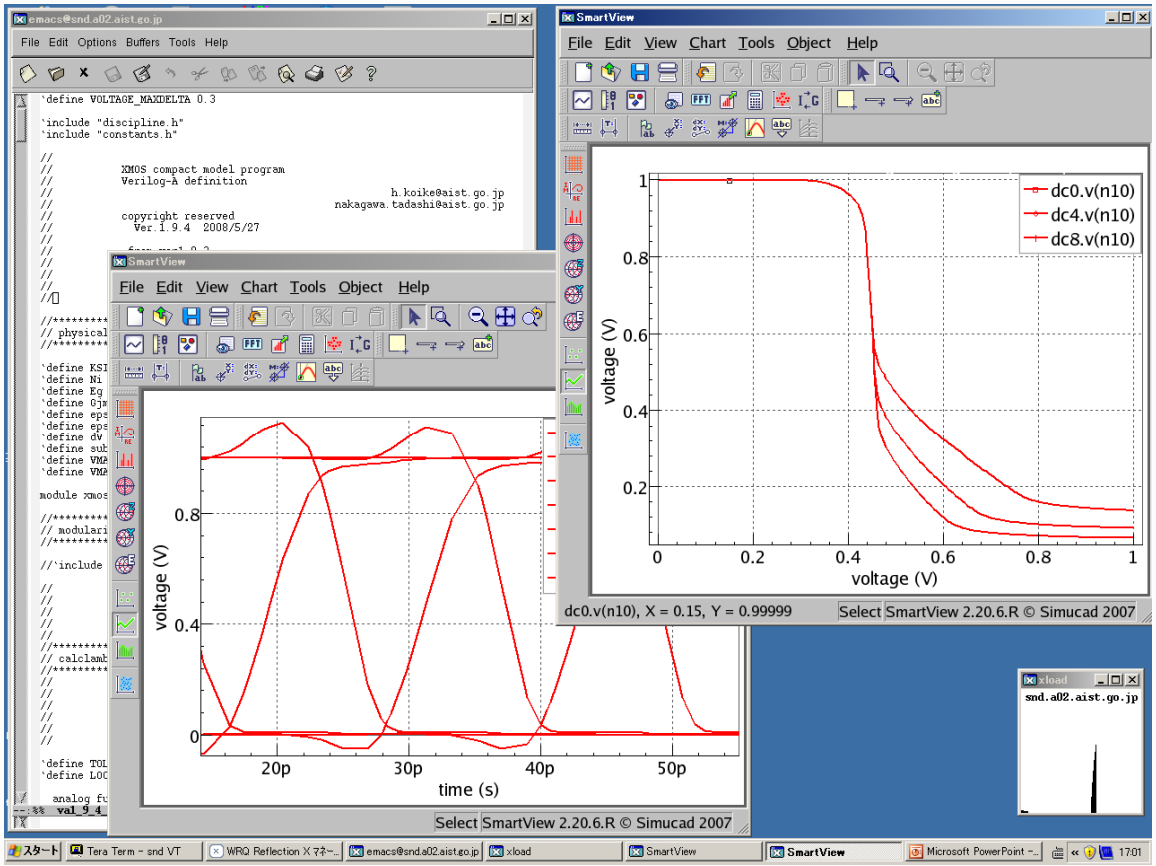


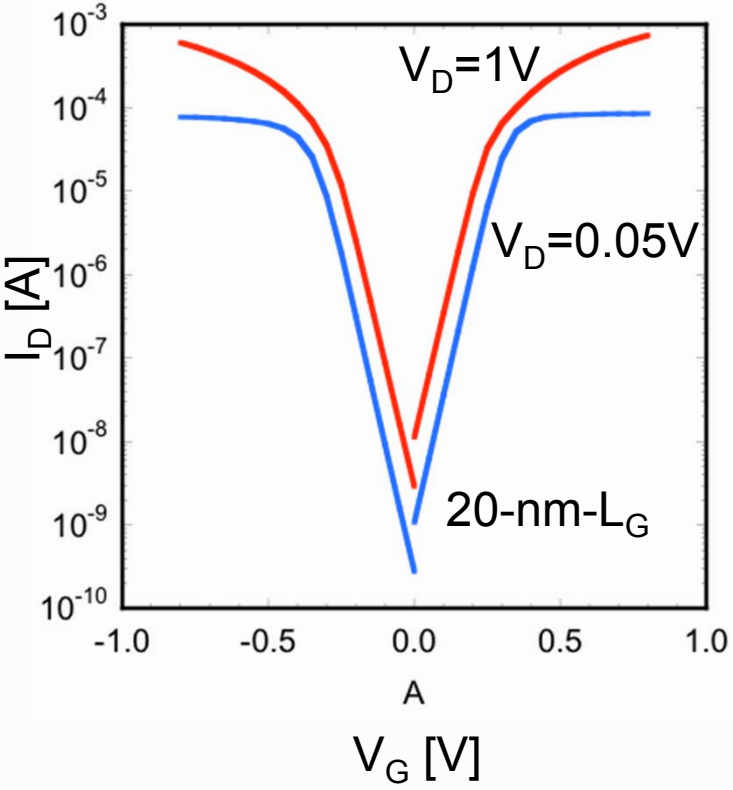
Flex-PG



- ✓Monte Carlo SPICE simulation using the FinFET compact model for 14- and 10-nm technology
- ✓Device parameters are from ITRS 2011

FinFET Compact Model (AIST)

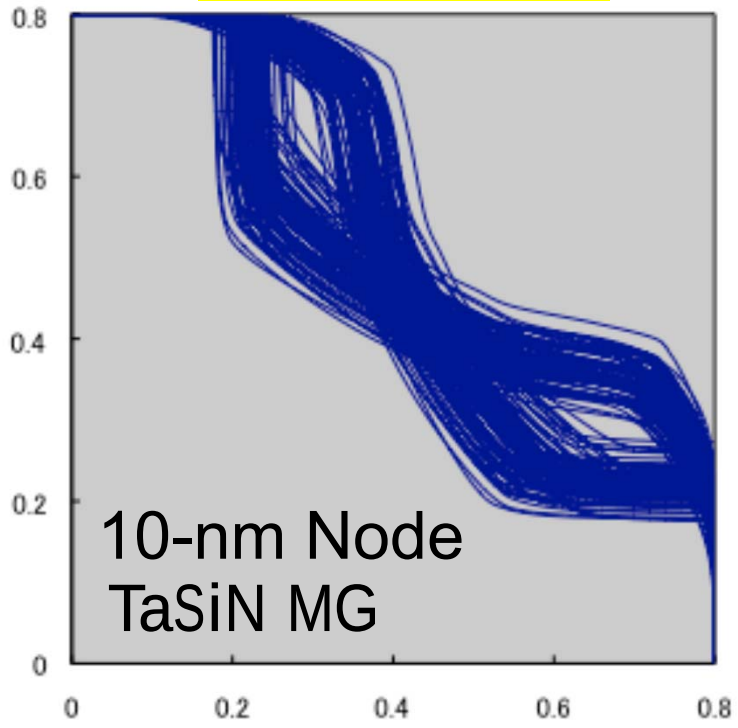




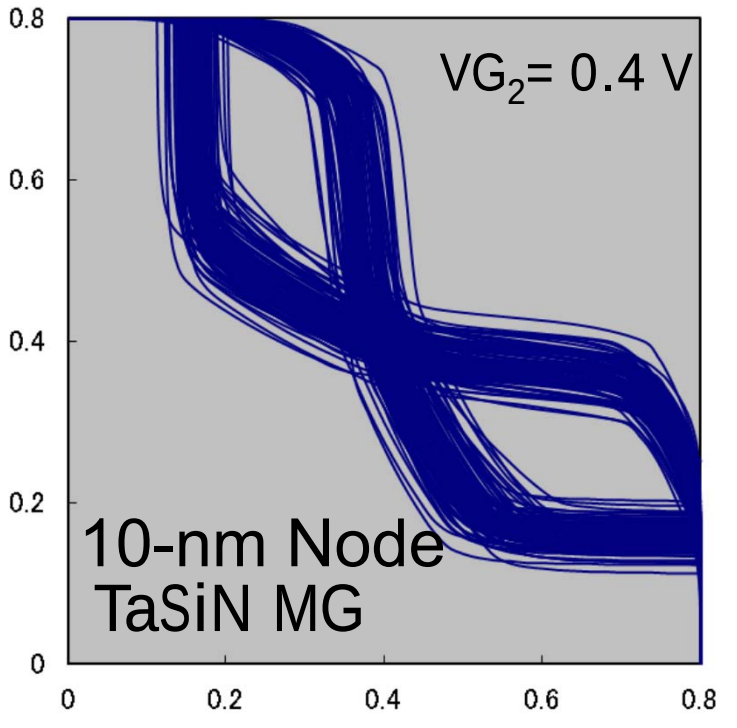
T. Nakagawa, et al., (AIST), IWCM, 2008
S. Ouchi, et al., (AIST) IEDM, 2008, p.709

SRAM Butterfly Curves

Common-DG

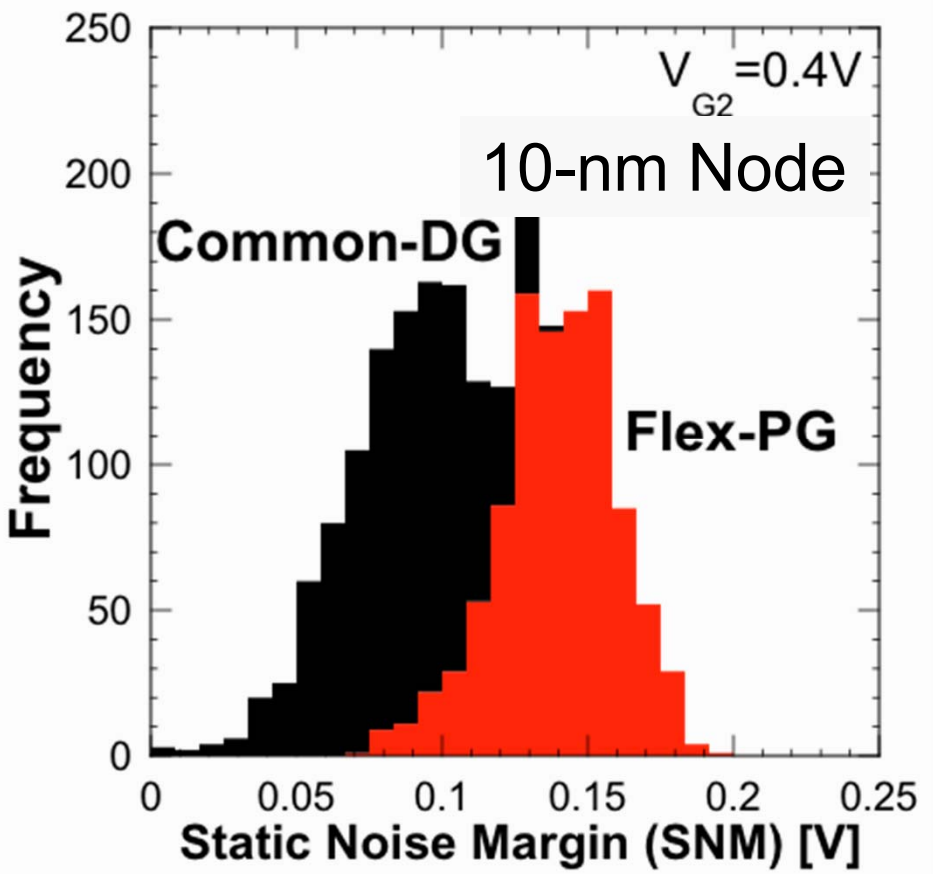


Flex-PG



✓ **Common-DG SRAM suffers form variability in spite of TaSiN MG**

Simulated Results (10-nm Node)



TaSiN
Avt =1.34

✓ **Flex-PG and amorphous TaSiN enables 10-nm SRAM cell with sufficient margin.**

Summary

- ✓ Reduction of the WFV has been successfully demonstrated.
- ✓ Independent-DG FinFET have been introduced into the SRAM cell to enhance performance.
- ✓ The device and circuit collaboration enables the 10-nm SRAM cell and beyond with sufficient margin.

Acknowledgement

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